DETAILED ACTION

1. Claims 1, 4, and 7-9 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 7/23/2009.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 4, and 7-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the examiner has been unable to find support in the original disclosure for the built-in processor using the processor bus and the second interface of the cross-bar switch, without stopping an operation of the external processor. Applicant is asked to point the examiner to specific portions of the specification and drawings which show support for such features set forth in claim 1. Otherwise, they should be canceled from claim 1.

5. Claims 4 and 7-9 are rejected under 35 U.S.C. 112, 1st paragraph, for lacking written description, because they are each dependent on a claim lacking written description.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto, U.S. Patent No. 4,065,809, in view of Guttag, U.S. Patent No. 4,521,852. In addition, Yabushita et al., U.S. Patent No. 5,214,775 (herein referred to as Yabushita), is herein used as extrinsic evidence for showing that processors on separate chips may share a memory found on one of the chips.

8. Referring to claim 1, Matsumoto has taught a processor system comprising:

a) a single semiconductor substrate on which is provided a built-in processor (Fig.1, component 11), a memory controller (a system with memory inherently has a memory controller to control accesses to the memory), and a connection unit that mutually connects the memory controller and a processor bus (a processor bus is inherently connected to memory via the memory controller so that instructions/data may be obtained for processing).

b) Matsumoto has taught a second processor on the substrate (Fig.1, component 12). Matsumoto has not taught that the single semiconductor substrate includes an external bus interface to which an external processor is connected from outside of the single semiconductor substrate, the processor bus being connected with the first processor and the external bus interface. However, Guttag has taught a chip including a built-in processor and an external bus interface through

which peripherals communicate with components on chip. See Fig.1 and column 3, line 41, to column 4, line 39. The examiner asserts that any parts may be integrated on a single chip or made separate, as integration and separation of parts are well known and not patentable features. See *In re Larson 144 USPQ 347 (CCPA 1965)* and *Nerwin v. Erlichman 168 USPQ 177 (1969)*. As a result, since separation of parts is a non-patentable feature, it would have been obvious to one of ordinary skill in the art to modify Matsumoto in view of Guttag such that the single semiconductor substrate includes an external bus interface to which the second processor (Matsumoto, Fig.1, component 12) is connected from outside of the single semiconductor substrate, the processor bus being connected with the first processor and the external bus interface. It should be noted that, while Guttag does not explicitly disclose that a peripheral is an external processor, it is known that an external processor can access another processor's on-chip memory. For instance, see Yabushita, Fig.1, Fig.10, the abstract, column 2, lines 65-68, and claim 11, which provides a specific teaching of a processor and shared memory on a single chip and a processor external to the chip which communicates with the shared memory via an external interface. Hence, given each of these teachings, separating processor 12 of Matsumoto out onto another chip and allowing it to access the memory 19 through an external bus interface would have been obvious.

c) Matsumoto, as modified, has not taught that the connection unit is a cross-bar switch comprising at least a first interface connected to the memory controller and a second interface connected to the processor bus. However, crossbar switches and their advantages are well known and accepted in the art. A crossbar switch is useful because as the traffic between any two devices increases, it does not affect traffic between other devices. In addition, it is much

more scalable than a traditional bus. Consequently, to reduce traffic and increase scalability, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto such that the connection unit is a crossbar switch with interfaces coupled to the bus and memory controller.

d) Matsumoto, as modified, has further taught that first and second signal lines for inputting first and second enable signals are connected to reset signal lines of the built-in processor and the external bus interface, respectively, wherein the first enable signal is asserted while the second enable signal is deasserted, so that the built-in processor is in a reset state to suppress issuance of a request for using the processor bus from the built-in processor and the external bus interface can use the processor bus and the second interface of the cross-bar switch exclusively, and wherein the second enable signal is asserted while the first enable signal is deasserted, so that the external bus interface is in a reset state to suppress issuance of a request for using the processor bus from the external bus interface and the built-in processor can use the processor bus and the second interface of the cross-bar switch exclusively, without stopping an operation of the external processor. See Fig.1 and the abstract of Matsumoto, and note the WAITa and WAITb signals. Also, see column 4, lines 56-63, and column 6, lines 42-48. When one WAIT signal is asserted the other is deasserted so that there is no bus contention between two processors when a memory access is requested. Note that Matsumoto, as modified in view of Guttag, would send the WAITb signal to the external bus interface, much like the inhibit signal of Guttag is sent to the external bus interface in Fig.1, so that the peripheral processor's request to communicate on-chip is either granted or suppressed. Furthermore, from Fig.2 and column 7, lines 32-35. When

a processor is forced to wait, it may still generate a memory access cycle signal. Hence, the waiting processor is not stopped from performing an operation.

9. Referring to claim 7, Matsumoto, as modified, has taught the processor system according to claim 1, wherein the built-in processor and the external bus interface are connected through a bus common to the cross-bar switch. See Fig.1 of Guttag, and recall that when Matsumoto is modified to include the external bus interface, such a common bus would exist in order to share memory accesses on a single bus, as set forth in Matsumoto.

10. Claims 4 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Guttag, and further in view of the examiner's taking of Official Notice.

11. Referring to claim 4, Matsumoto, as modified, has taught the processor system according to claim 1. Matsumoto, as modified, has not taught a second built-in processor connected to the cross-bar switch on the semiconductor substrate. However, systems having multiple processors or being scaled to include multiple processors is known in the art and advantageous because more processors yield more processing power, and throughput. Consequently, in order to increase performance, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto to include a second built-in processor connected to the connection unit on the semiconductor substrate.

12. Referring to claim 8, Matsumoto, as modified, has taught the processor system according to claim 1. Matsumoto, as modified, has not taught that the built-in processor and the external processor use in common programs stored in a memory controlled by the memory controller. However, it is knows that a single program may be broken up into pieces to be executed by

multiple processors, thereby speeding up execution of that single program. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto such that the built-in processor and the external processor use in common programs stored in a memory controlled by the memory controller.

13. Referring to claim 9, Matsumoto, as modified, has taught the processor system according to claim 1. Matsumoto, as modified, has not taught an image data transfer bus connected with the cross-bar switch, nor has Matsumoto, as modified, taught an image output device interface or an image input device interface connected with the image data transfer bus on the semiconductor substrate. However, image processing is well known in the art, and in order to obtain image processing functionality in the system of Matsumoto, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Matsumoto to include an image data transfer bus and an image output device interface or image input device interface so that images may be transferred to and from the processor for or after processing.

Response to Arguments

14. Applicant's arguments filed on July 23, 2009, have been fully considered but they are not persuasive.

15. Applicant appears to be arguing on page 11, of the remarks, that amended claim 1 overcomes Matsumoto because Matsumoto has not taught "...without stopping an operation of the external processor." However, as described in the rejection above, Matsumoto at least allows a memory access cycle signal generation operation to occur while the processor is waiting. Hence, an operation of the processor is not stopped. See column 7, lines 32-35.

16. On page 12 of the remarks, regarding applicant's traversal of the examiner's taking of Official Notice to reject claim 1, MPEP 2144.03 states that " To adequately traverse such a finding, an applicant must specifically point out the supposed errors in the examiner's action, which would include stating why the noticed fact is not considered to be common knowledge or well-known in the art. See 37 CFR 1.111(b)." Such reasoning has not been provided by applicant. Therefore, the examiner hereby requests applicant provide reasoning why using a well-known crossbar structure is a concept that is not well known in the art and not advantageous. However, even if applicant did supply such reasoning, applicant's attention is directed to Noel, U.S. Patent No. 6,557,070 (column 1, lines 19-48) and the attached definition, which despite being from 2007, sets forth the known definition of crossbar. Essentially, they teach that crossbars are scalable and that they are efficient in handling traffic. As a result, the examiner asserts that the Official Notice that crossbars are well known and advantageous is supported.

17. On page 12, applicant argues that "even if such a cross-bar switch were somehow used in the system disclosed by Matsumoto, Applicant respectfully submits that the combination would still fail to teach the claimed arrangement. In particular, Claim 1 recites a cross-bar switch with two interfaces, in which the same interface of the cross-bar switch is shared via a common processor bus by the external processor and the built-in processor. Accordingly, Applicant respectfully submits that even if Matsumoto was modified to include a cross-bar switch, the combination would fail to teach the claimed utilization of two interfaces thereof, in which a first

interface is connected to a memory controller and a second interface is shared via a common processor bus by an external processor and a built-in processor". However, the examiner asserts that the same interface is shared by the processors. See Fig.1 and note that both the RAMC interface is shared by both processors. This is the reason that the wait signals are required. They can't both access a single interface at once.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183